## Sample Problem \#1

- We have a machine with 4 GiB of RAM
- We have a page size of 8 KiB
- We allow processes to have 1GiB address spaces
- How many bits are used for physical addresses?
- How many bits are used for logical addresses?
- How many bits are used for logical page numbers?


## Sample Problem \#2

- 32-byte memory
- 16-byte address space
- 4-byte pages
- 4-bit logical addresses
- 5-bit physical addresses

| 0 | $a$ |
| :---: | :---: |
| 1 | b |
| 2 | c |
| 3 | d |
| 4 | e |
| 5 | f |
| 6 | g |
| 7 | h |
| 8 | i |
| 9 | j |
| 10 | k |
| 11 | l |
| 12 | m |
| 13 | n |
| 14 | o |
| 15 | p |

- What is the physical address corresponding to logical address 6 ?

page table
logical memory

| 0 |  |
| :---: | :---: |
| 4 | $\begin{aligned} & \mathrm{i} \\ & \mathrm{j} \\ & \mathrm{k} \end{aligned}$ |
| 8 | $\begin{aligned} & \mathrm{m} \\ & \mathrm{n} \\ & \mathrm{o} \\ & \mathrm{p} \end{aligned}$ |
| 12 |  |
| 16 |  |
| 20 | $\begin{aligned} & \hline a \\ & b \\ & c \\ & c \end{aligned}$ |
| 24 | $\begin{aligned} & \mathrm{e} \\ & \mathrm{f} \\ & \mathrm{~g} \\ & \mathrm{~h} \\ & \hline \end{aligned}$ |
| 28 |  |

physical memory

## Sample Problem \#3

- Page size: 32 KiB
- Logical addresses: 39 bits
- Page table entry size: 8 bytes
- Question: using 2-level paging, how is a logical address split into its 3 components (p1, p2, offset)?

